REMARKS

Applicants note with appreciation the indication of allowable subject matter in the instant application, namely, the subject matter recited in Claims 2-11 and 13-24. Now in the application are Claims 1-24 of which Claims 1 and 12 are independent. The following comments address all stated grounds for rejection, and place the presently pending claims, as identified above, in condition for allowance.

Claim Rejections under 35 USC § 102

Claims 1 and 12 stand rejected under 35 U.S.C. § 102(a). For ease of the discussion below, the rejection of Claims 1 and 12 under 35 U.S.C. § 102(a) are discussed separately.

A. Rejection of Claim 1 under 35 U.S.C. 102(a):

Claim 1 stands rejected under 35 U.S.C. § 102(a) as being anticipated by U.S. Patent No. 6,570,944 of Best, *et al.* (hereinafter "Best"). Applicants respectfully traverse this rejection and contend that Best does not anticipate Claim 1.

Claim 1 is directed to an apparatus for receiving data of a source synchronous signal and a source synchronous clock signal in a source synchronous point to point communication system. The apparatus includes a receiver circuit for receiving the data of the source synchronous signal and a feedback circuit for providing the receiver with a number of feedback signals based on an output of the receiver circuit to synchronize receipt of the data of the source synchronous signal by the receiver circuit. The Best patent does not anticipate Claim 1. The Best patent is directed to clock generation for a high speed data link. More specifically, the Best patent discloses a dual loop phase lock loop (PLL) architecture to generate a quadrature clock signal for sampling data received on receiver (130). The dual loop architecture taught by Best combines a core loop (102) to generate a set of closely spaced clocks with a peripheral loop (112) that interpolates between these clocks. The core loop and peripheral loop can decouple frequency and phase acquisition and enable the construction of a DLL with an infinite phase range. The peripheral loop (112) acquires phase under the control of the phase detector (120) with digital control (122). The resulting output signal of this dual loop architecture is a quadrature clock signal DSS1 received on a first input of the receiver (130) for use in sampling data signal DQ1.

In operation, the receiver (130) uses the clock signal DSS1 to sample data DQ1 received on a second input of the receiver. Nevertheless, the architecture, operation, and function of the clock circuit and receiver circuit disclosed by Best differs from the apparatus recited in Claim 1 because the Best reference does not provide feedback to the receiver (130) based on the output of the said receiver.

In contrast to the apparatus of Claim 1, the architecture disclosed by Best provides feedback only to the clock generation circuit or the dual loop architecture via the comparison of the phase lock signal (PL) with the strobe signal (DQS) by the zero phase detector (120). That is, the architecture, operation, and function of the clock generation circuit disclosed by Best does not provide a plurality of feedback signals based on an output of the receiver circuit to synchronize receipt of the data of the source synchronous signal by the receiver circuit. In fact, the receiver (130) of Best does not receive any feedback signal and only receives a data signal DQ and a clock signal DSS used for sampling the data signal. Hence, Best does not anticipate Claim 1.

For at least these reasons, Applicants respectfully contend the Best reference does not anticipate Claim 1. Applicants respectfully request the Examiner to reconsider and withdraw the rejection of Claim 1 under 35 U.S.C. 102(a).

B. Rejection of Claim 12 under 35 U.S.C. § 102(a):

Claim 12 stand rejected under 35 U.S.C. § 102(a) as being anticipated by Best. Applicants respectfully traverse this rejection and contend that Best does not anticipate Claim 12.

Claim 12 is directed to a method for continuously synchronizing a source synchronous clock signal on a clock line with a data signal on a data line at a receiver of the source synchronous clock signal and the data line. The method includes the step of determining at the receiver a phase relationship between the source synchronous clock signal and the data signal each time the receiver receives the source synchronous clock signal. The method also includes the step of synchronizing the source synchronous clock signal and the data signal to be in phase at the receiver each time the receiver receives the data signal and the source synchronous clock

signal. The synchronization is based on the determined phase relationship between the source synchronous clock signal and the data signal to continuously synchronize the source synchronous clock signal and the data signal to allow the receiver to integrate the data signal over an entire period of the clock signal. The Best patent does not anticipate Claim 12.

As discussed above in relation to the rejection of Claim 1, the Best patent discloses a dual loop clock generation architecture which supplies a quadrature clock signal to a receiver for use in sampling a received data signal on a data line DQ1. The Best reference does not disclose synchronizing the source synchronous clock signal and the data signal to be in phase at the receiver each time the receiver receives the data signal and the source synchronous clock signal. More specifically, the receiver (130) of Best does not receive the source synchronous clock signal. Further, the Best patent teaches the source synchronous clock signal is synchronized with a phase lock signal (PL) generated by the dual loop clock generation architecture. Hence, Best discloses synchronizing two clock signals and does not disclose synchronizing a data signal and a clock signal as recited in the method of Claim 12. Thus, Best does not anticipate Claim 12.

For at least these reasons, the Best reference does not detract from the patentability of Claim 12. Accordingly, Applicants respectfully request the Examiner to reconsider and withdraw the rejection of Claim 12 under 35 U.S.C. § 102(a).

CONCLUSION

In view of the above amendment, applicant believes the pending application is in condition for allowance.

Applicant believes no fee is due with this statement. However, if a fee is due, please charge our Deposit Account No. 12-0080, under Order No. SMQ-068 from which the undersigned is authorized to draw.

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Respectfully submitted,

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